In re Patent Application of   )
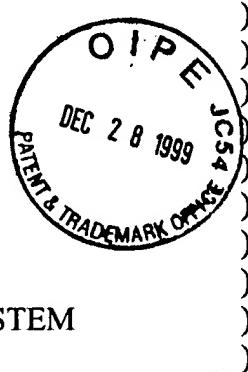
ELIYAHOU HARARI et al.   )

Serial No.: 08/789,421   )

Filed: January 29, 1997   )

For: FLASH EEPROM SYSTEM   )

Group Art Unit: 2785

San Francisco, California

Assistant Commissioner of Patents
Washington, D.C. 20231

PRELIMINARY AMENDMENT

Sir:

Please amend certain of the claims of the recently filed Second Continued Prosecution
Application, as follows:

63. (Thrice Amended) A method of operating a bulk storage memory with a
host processor, wherein the bulk storage memory includes an array of non-volatile floating gate
memory cells, comprising:

storing, within defined non-overlapping groups of said array cells, sectors of user data
and associated overhead data, at least some of said overhead data being generated within the bulk
storage memory to include information of at least one of (a) the same individual memory array cell
groups in which the overhead data are stored or (b) the user data stored in the same individual
memory array cell groups as the overhead data,

in response to receipt from the host processor of an address in a format designating
at least one mass memory storage block address, converting said at least one mass memory storage
block address into an address of at least one of the memory array cell groups and addressing said at
least one of the memory array cell groups,